

Abstract of cited reference 1.

Title : The electronic cycle computer for bicycle
Filing date: Jun 17, 1997
Application No.: 87217502 (Utility Model Patent)
Publication date: January 11, 2000
Publication No: 379806
Creators : Watari I Etsuyoshi (Japanese), Chun-Mu Hwang
Applicant : Shimano Co., Limited. (Japan)
Ming-shih electronic enterprise Limited Co.
Patent attorney: Chih-Kang Lin

Related claims:

Claim 1 : A electronic cycle computer for bicycle, comprises: the main body of cycle computer with microprocessor and display device, and the bracket which can be installed on the bicycle and provides the said cycle computer main body installed on it in assemble/dismount conveniently fashion, the plural sensors which be installed on the bicycle could respective detect the said bicycle, and the signals transmission apparatus which transmits the output sensing signals to the mentioned cycle computer main body. Utilizing the said microprocessor processes the signals transmitted from the said sensors to identify, count and/or arithmetic operation, and then display on the said display device, characterized in, the said bracket with sub-microprocessor, the said sub-microprocessor connects with the said respective sensors by the said signal transmission means, receiving the output sensing signal of sensors in parallel signal, and then transfers to series signal, through the contacts which be installed on bracket electrically and connected to cycle computer main body transmits to the said microprocessor.

Brief description of the drawings:

Fig.1 : shown front view of prior technology for bicycle electronic cycle computer

Fig.2 : shown rear view of prior technology for bicycle electronic cycle computer

Fig.3 : shown side view for the state of installing the cycle computer main body on bracket

Fig.4 : shown the solid view of connection relationship between bracket and two sensors

Fig 5 : shown the side view of the installation method for wheel rotation number sensors which compose of magnet and magnetic sensors

Fig 6 : shown the side view of the installation method for treadle rotation number sensors which compose of magnet and magnetic sensors

Fig 7 : shown the dismount section view for water proof sealing structure of metal contact

Fig 8 : shown the main component block diagram for the bicycle electronic cycle computer of 1st embodiment for this invention

- Fig 9 : shown a group of data composed of series signals and the waveform of synchronized clock signals
- Fig 10 : shown the main component block diagram for the bicycle electronic cycle computer of 2nd embodiment for this invention
- Fig 11 : shown the main component block diagram for the bicycle electronic cycle computer of 3rd embodiment for this invention
- Fig 12 : shown the main component block diagram for the bicycle electronic cycle computer of 4th embodiment for this invention

Abstract of cited reference 2.

Title : Programmable VT time slots for SONET use

Filing date: April 12, 1996

Application No.: 85205258 (Utility Model Patent)

Publication date: September 1, 1996

Publication No: 285383

Creators : Yeong-Jiunn Chuang, Wu-Jyh Chiou, Jyi-Yuan Wu, Wan-Bin Shieh, Shlun-Cherng Li (all with Taiwanese nationality)

Applicant : Chunghwa Telecom Laboratories, Taiwan

Patent attorney: Jou-Feng Jiang

Related claims:

Claim 1 : A programmable VT time slots exchanger for SONET use, mainly includes VT time slots exchange unit, microprocessor interface unit, STS-1 (synchronize transmission signal) format recombination unit, POH (path additional signal) processing unit and time sequence generate unit; the VT time slots exchange unit executes all VT exchange functions, and then through STS-1 format recombination unit recombines to STS-1 signal of three way in series. The time sequence generate unit provides the necessary time sequence signal, and then the microprocessor unit gets exchange routing message and other control data which are requested by time slots unit through exterior microprocessor. The POH processing units executes monitoring and sampling for STS-3 input signal, and then storing error code accumulated value and received J1 byte into microprocessor interface unit at the same time.

Brief description of the drawings:

- Fig.1 : shown conception block diagram for time slots exchange of prior digital voice exchanger
- Fig.2 : shown block diagram for this creator
- Fig.3 : shown block diagram for VT time slots exchange unit of this creator
- Fig.4 : shown block diagram for STS-1 format recombination unit of this creator
- Fig 5 : shown the multiplex block diagram and time sequence for SUS-3 bus exterior three state for this creation
- Fig 6 : shown count flow chart view for read/write control unit counter of this creator

- Fig 7 : shown block diagram for SUS-3 bus to SUS-1 bus de-multiplex of this creator
- Fig 8 : shown conception view for microprocessor interface address arrangement of this creator
- Fig 9 : shown conception view for SONET VT DM application of this creator

BEST AVAILABLE COPY

中華民國專利公報 [19] [12]

[11]公告編號: 379806

[44]中華民國 89年(2000) 01月11日
新型

全 7 頁

[51] Int.Cl^{U6}: G01C22/00

[54]名 稱: 自行車電子碼錶

[21]申請案號: 087217502

[22]申請日期: 中華民國 86年(1997) 06月17日

[72]創作人:

渡會悅義

日本

黃榕木

台北縣三重市三和路四段八十五號

[71]申請人:

島野股份有限公司

日本

名世電子企業股份有限公司

台北縣三重市三和路四段八十五號

[74]代理人: 林志剛

先生

1

2

[57]申請專利範圍:

1.一種自行車電子碼錶(cycle computer),

係由:具備微處理器及顯示裝置的碼錶本體、及可安裝在自行車上,並供前述碼錶本體以拆裝自如方式安裝在其上的托架、及複數個安裝在該自行車上之可分別偵測該自行車上的察覺器、及將前述察覺器所輸出訊號傳輸到前述碼錶本體的訊號傳輸手段所組成,利用前述微處理器對於前述各察覺器所送來的訊號進行辨識、計數及/或運算處理後顯示於前述顯示裝置之形態的自行車電子碼錶,其特徵為:

前述托架內係設有副微處理器,該副微處理器係與前述各察覺器經由前述訊號傳輸手段相連接,以並列方式接收由前述各察覺器所輸出的偵測訊號後,將其轉換成串列方式的訊號,經由該托架上與前述碼錶主體電性連通的接點傳輸到前述微處理器。

2.一種自行車電子碼錶(cycle computer),

5.

10.

15.

20.

係由:具備微處理器及顯示裝置之可安裝於自行車上的碼錶本體、及複數個安裝在該自行車上之可分別偵測該自行車上的察覺器、及將前述察覺器所偵測的訊號供給到前述碼錶本體的訊號傳輸手段所組成,利用前述微處理器對於前述各察覺器所送來的訊號進行辨識、計數及/或運算處理後顯示於前述顯示裝置之形態的自行車電子碼錶,其特徵為:
該自行車電子碼錶另具有:設於前述自行車車體上的副微處理器,該副微處理器係與前述各察覺器經由前述訊號傳輸手段相連接,以並列方式接收由前述各察覺器所輸出的偵測訊號後,將其轉換成串列方式的訊號,經由該副微處理器與前述微處理器之間的訊號傳輸線傳輸到前述微處理器。

3.一種自行車電子碼錶(cycle computer),
係由:具備微處理器及顯示裝置的碼錶本體、及可安裝在自行車上,並供前述

(2)

3

碼錶本體以拆裝自如方式安裝在其上的托架、及複數個安裝在該自行車上之可分別偵測該自行車上的察覺器、及將前述察覺器所輸出訊號傳輸到前述碼錶本體的訊號傳輸手段所組成，利用前述微處理器對於前述各察覺器所送來的訊號進行辨識、計數及／或運算處理後顯示於前述顯示裝置，前述微處理器並可根據運算處理的結果，輸出變速控制訊號到電子式自動變速器以令其進行變速之形態的自行車電子碼錶，其特徵為：前述托架內係設有副微處理器，該副微處理器係與前述各察覺器經由前述訊號傳輸手段相連接，以並列方式接收由前述各察覺器所輸出的偵測訊號後，將其轉換成串列方式的訊號，經由該托架上與前述碼錶主體電性連通的接點傳輸到前述微處理器，而前述微處理器所輸出的前述控制訊號也是經由前述接點傳輸到前述副微處理器後，再傳輸到前述電子式自動變速器。

- 4.一種自行車電子碼錶(cycle computer)，係由：具備微處理器及顯示裝置之可安裝於自行車上的碼錶本體、及複數個安裝在該自行車上之可分別偵測該自行車上的察覺器、及將前述察覺器所偵測的訊號供給到前述碼錶本體的訊號傳輸手段所組成，利用前述微處理器對於前述各察覺器所送來的訊號進行辨識、計數及／或運算處理後顯示於前述顯示裝置，前述微處理器並可根據運算處理的結果，輸出變速控制訊號到電子式自動變速器以令其進行變速之形態的自行車電子碼錶，其特徵為：該自行車電子碼錶另具有：設於前述自行車車體上的副微處理器，該副微處理器係與前述各察覺器經由前述訊號傳輸手段相連接，以並列方式接收由前述各察覺器所輸出的偵測訊號後，將其轉換

4

成串列方式的訊號，經由該副微處理器與前述微處理器之間的訊號傳輸線傳輸到前述微處理器。

而前述微處理器所輸出的前述控制訊號也是經由前述訊號傳輸線傳輸到前述副微處理器後，再傳輸到前述電子式自動變速器。

5. 如申請專利範圍第1、2、3或4項之自行車電子碼錶，其中復具有：與前述碼錶本體分開之可另設於自行車車把上，利用訊號傳輸線與前述副微處理器相連接，並可對於前述微處理器進行遙控操作、設定資料的遙控操作鍵。
10. 如申請專利範圍第1、2、3或4項之自行車電子碼錶，其中前述複數個察覺器係包含：用以偵測自行車的車輪迴轉數、踏板迴轉速、變速器檔位之類的各種資訊及／或安裝在騎乘者身上以偵測該騎乘者的各種生理狀態資訊的各種察覺器中的至少兩種。
15. 如申請專利範圍第6項之自行車電子碼錶，其中由前述顯示裝置所顯示的資訊為：車速資訊、踏板迴轉速資訊、變速器檔位資訊、時間資訊、行車旅程資訊、騎乘者的生理狀態資訊的其中一種或者同時顯示其中兩種以上的資訊。
20. 圖式簡單說明：
- 第一圖是先前技術的自行車電子碼錶的正面圖。
25. 第二圖是先前技術的自行車電子碼錶的背面圖。
30. 第三圖是顯示將碼錶本體插裝在托架上的狀態的側面圖。
35. 第四圖是顯示托架與兩個察覺器的連結關係的立體圖。
- 第五圖是顯示由磁鐵與磁性察覺器所組成的車輪迴轉數察覺器的安裝方式的側面圖。
40. 第六圖是顯示由磁鐵與磁性察覺器所組成的踏板迴轉速察覺器的安裝方式的

(3)

5

側面圖。

第七圖是顯示金屬接點的防水密封結構的分解斷面圖。

第八圖是顯示本創作的第1實施例的自行車電子碼錶的構成要件的方塊圖。

第九圖是顯示由串列訊號所組成的一組資料與同步時鐘訊號的波形圖。

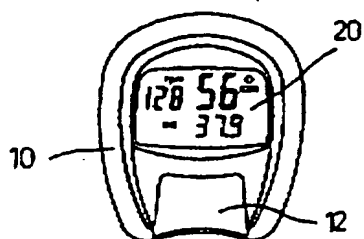
第十圖是顯示本創作的第2實施例

6

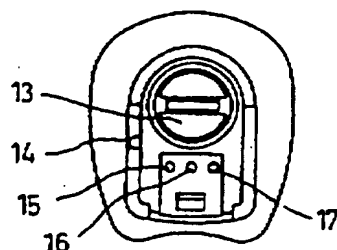
的自行車電子碼錶的構成要件的方塊圖。

第十一圖是顯示本創作的第3實施例的自行車電子碼錶的構成要件的方塊圖。

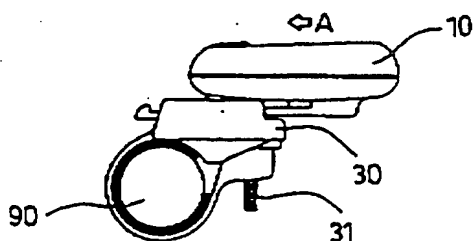
5. 第十二圖是顯示本創作的第4實施例的自行車電子碼錶的構成要件的方塊圖。



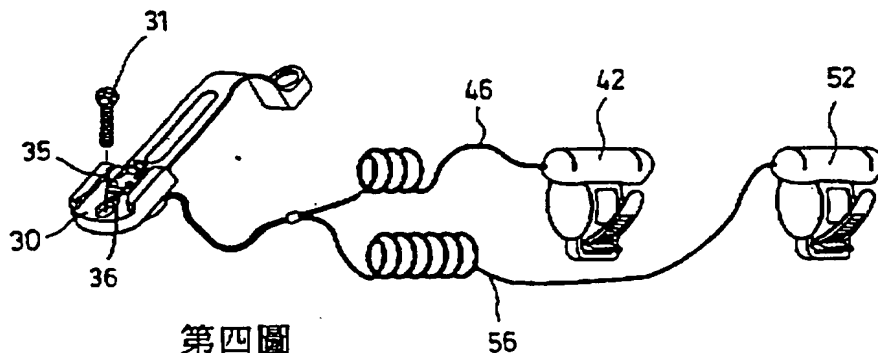
第一圖
(Fig. 1)



第二圖
(Fig. 2)

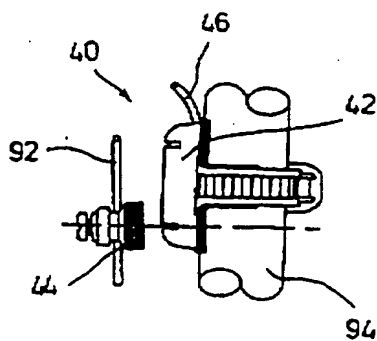


第三圖
(Fig. 3)

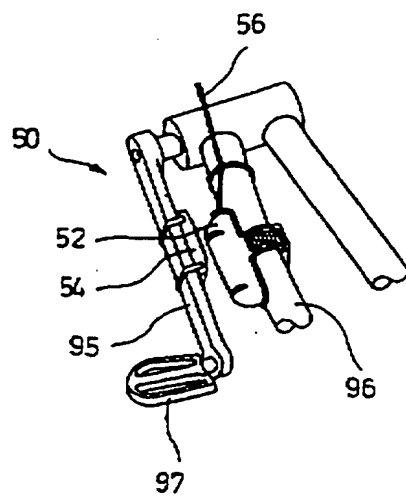


第四圖
(Fig. 4)

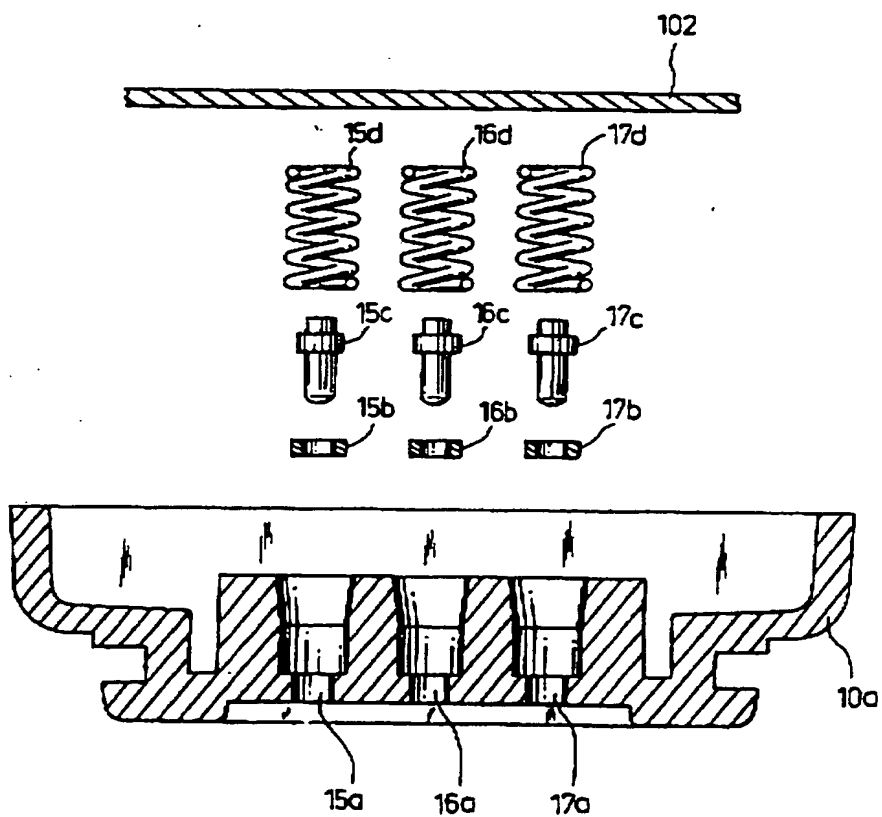
(4)



第五圖
(Fig. 5)

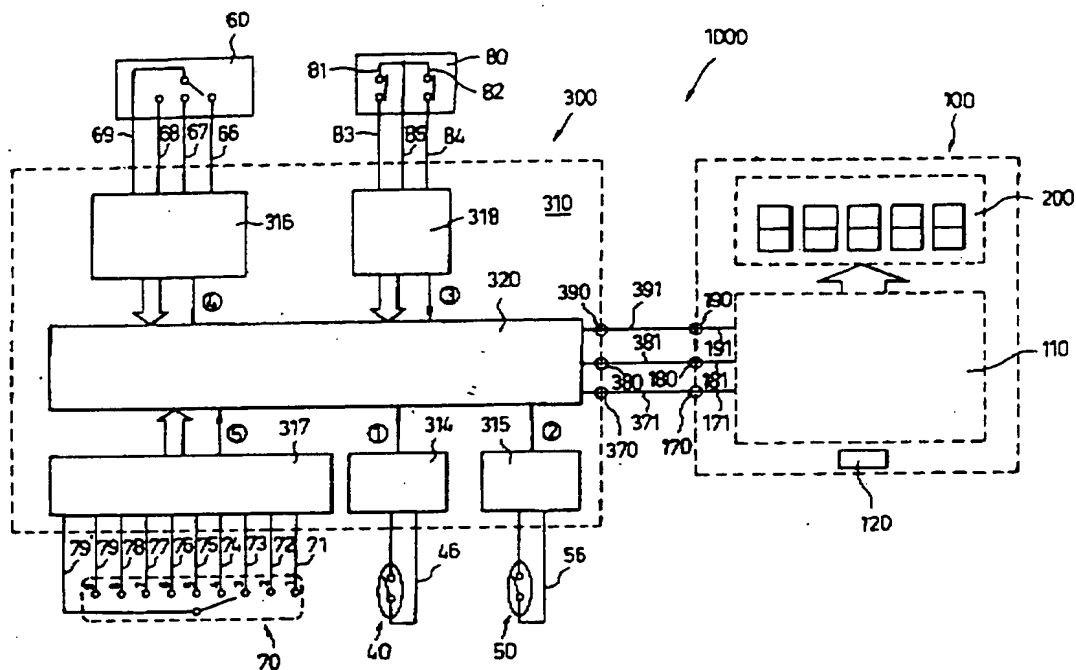


第六圖
(Fig. 6)

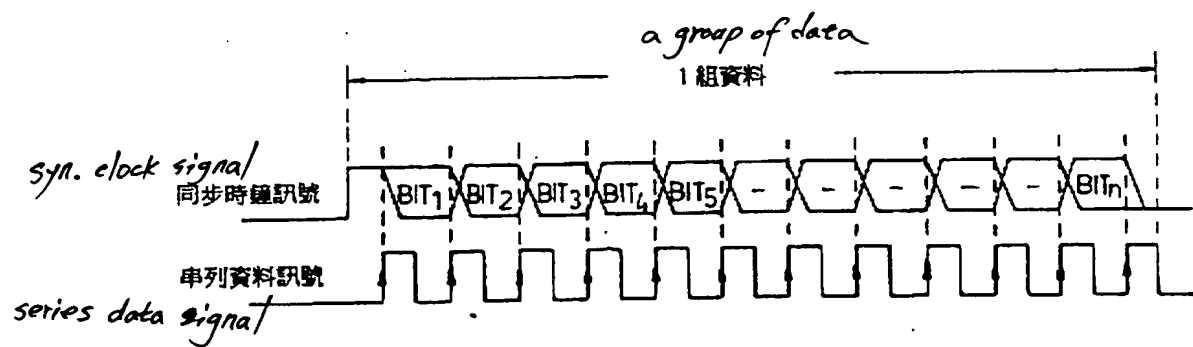


第七圖
(Fig. 7)

(5)

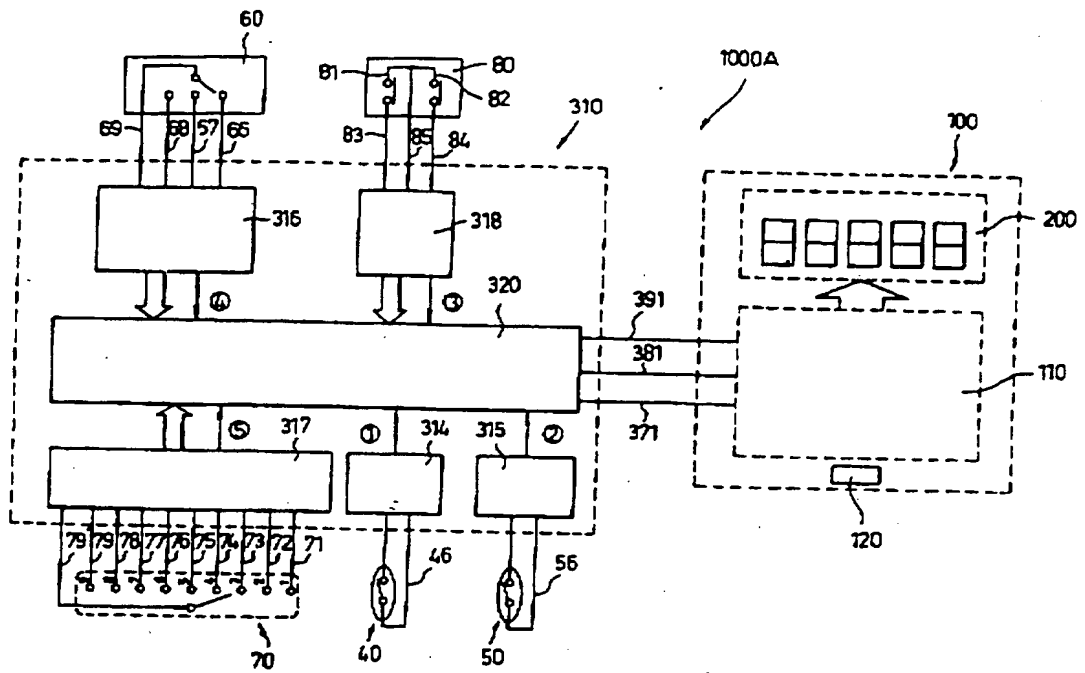


第八圖
(Fig. 8)

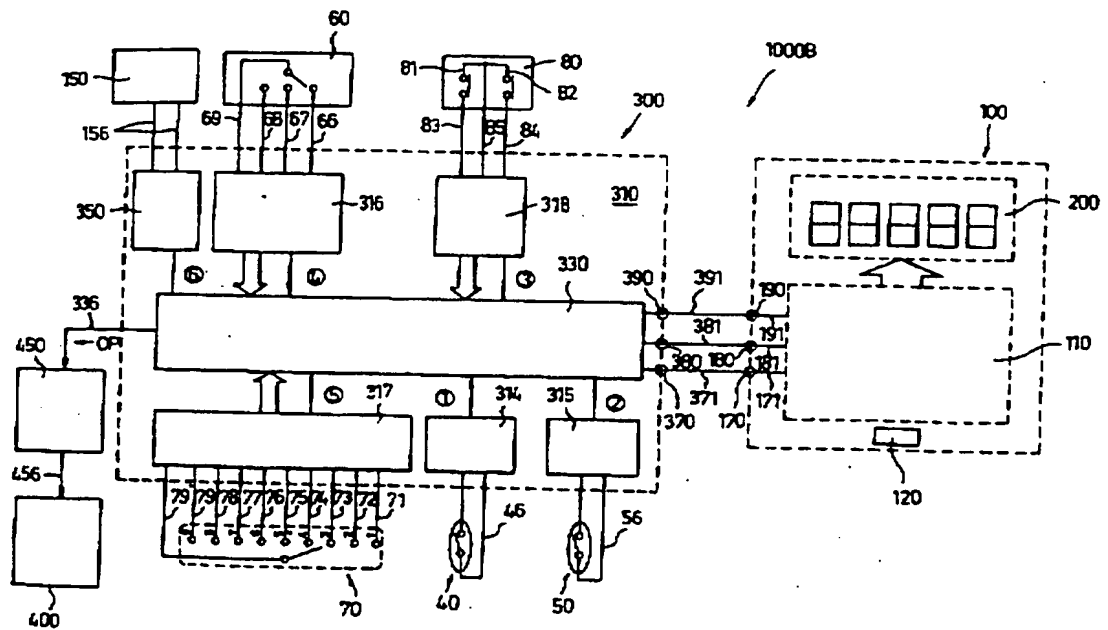


第九圖
(Fig. 9)

(6)

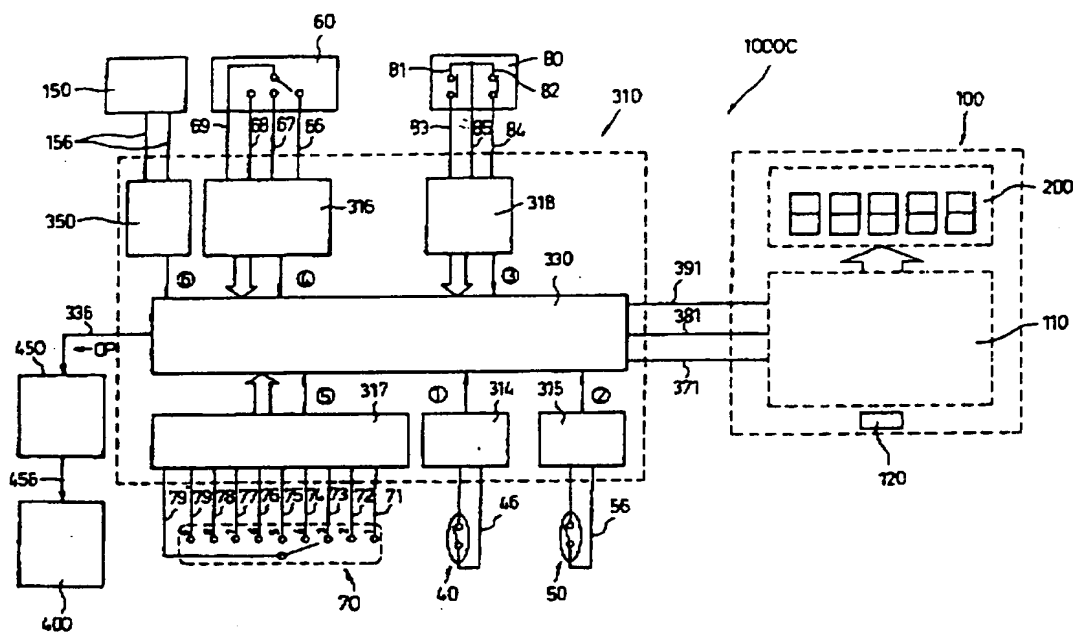


第十圖
(Fig. 10)



第十一圖
(Fig. 11)

(7)



第十二圖
(Fig. 12)

**This Page is Inserted by IFW Indexing and Scanning
Operations and is not part of the Official Record**

BEST AVAILABLE IMAGES

Defective images within this document are accurate representations of the original documents submitted by the applicant.

Defects in the images include but are not limited to the items checked:

- ☐ BLACK BORDERS
- ☐ IMAGE CUT OFF AT TOP, BOTTOM OR SIDES
- ☐ FADED TEXT OR DRAWING
- ☐ BLURRED OR ILLEGIBLE TEXT OR DRAWING
- ☐ SKEWED/SLANTED IMAGES
- ☐ COLOR OR BLACK AND WHITE PHOTOGRAPHS
- ☐ GRAY SCALE DOCUMENTS
- ☐ LINES OR MARKS ON ORIGINAL DOCUMENT
- ☐ REFERENCE(S) OR EXHIBIT(S) SUBMITTED ARE POOR QUALITY
- ☐ OTHER: _____

IMAGES ARE BEST AVAILABLE COPY.

As rescanning these documents will not correct the image problems checked, please do not report these problems to the IFW Image Problem Mailbox.